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Control of a resonant d.c.-link converter for a.c. motor drives

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This paper presents the control of the resonant d.c.-link converter for a.c. motor drives. This is a low loss converter with higher efficiency than a conventional PWM converter, but it requires complex control. It needs a special control of the resonant d.c.-link voltage in addition to the discrete control of the a.c. side currents. Simulations show how the control of the a.c. currents, the modulation principle, influences the overall performance of the converter.

1. Introduction

In order to control the torque and thus the speed of an a.c. motor, the motor needs a power supply which is able to supply a voltage or current with varying amplitude and frequency. This means that it is necessary to have a converter between the mains and the motor. The simplest and most commonly used converter is the hard switched pulse width modulated (PWM) converter.

This paper describes the resonant d.c.-link (RDCL) converter as an alternative to the PWM converter. It focuses on different current control methods. Computer simulations illustrate the special behaviour and complexity of this converter as well as its performance.

The RDCL converter is a low loss converter which requires special and complex control. It may be an alternative to the PWM converter in some special medium and small a.c. motor drives in the range of 10–100 kW. Examples are in applications where the gain from low acoustic noise and sinusoidal mains current can compensate for the complex control and high d.c.-link voltage.

Due to low transistor switching losses, a switching frequency above the audible level is possible. The low switching losses also make it possible to achieve sinusoidal mains current with low additional costs. This is important in surroundings where a large part of the main load is rectifiers.

2. Power conversion

2.1. *The conventional hard switching PWM converter*

Figure 1 shows a conventional converter with a diode rectifier, a constant d.c.-link voltage, V_{dc}, and a switched inverter. With the constant d.c.-link voltage, the amplitude and frequency of the output a.c. voltage is decoupled from the fixed amplitude and frequency of the input mains voltage. The output line motor voltages are generated as pulse trains with $+V_{dc}$, zero and $-V_{dc}$ as possible voltage values.

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The three phase inverter in Fig. 1 consists of three vertical bridge legs each with two switching transistors and two diodes. The transistors in the inverter are controlled to be either on, with full current and no voltage, or off, with no current and full voltage. One and only one of the transistors in a bridge leg is on at any time. When transistor $T1p$ is on, then v_1 equals $V_{d.c.}$ and when T 1n is on, then v_1 equals zero.

In the conventional pulse width modulated (PWM) inverter, the transistors will be switched each time the controller demands a new condition. The pulse width is chosen by the controller, only restricted by minimum on and off times. The transistor switching frequency, which is the frequency of each switching period including one on pulse and one off pulse, is also given by the controller.

In hard switching the switchings are accomplished with full current and voltage. When turning off the transistor, the voltage across it has to rise before the transistor current can start decreasing. In turn-on the transistor current builds up before the transistor voltage starts decreasing. These ideal turn-on and turn-off waveforms are shown in Fig. 2(*a*).

Figure 2(*b*) shows realistic transistor current and voltage switching waveforms and illustrates the problem of high frequency hard switching converters. That is the high switching losses due to the slow switchings on one hand, and on the other hand unacceptable high current and voltage stresses if the switchings are too fast.

Modern power transistors switch very fast. Still the switchings take time and cause power dissipation inside the switching element. The total switching losses are proportional to the switching frequency and become troublesome at high switching frequencies. In medium converters using the new fast switching IGBT transistors, a switching frequency above the audible level (15–20 kHz) is not possible to achieve without a considerable derating of the switching devices.

The strides in the development of power semiconductors have resulted in the production of faster and faster switching transistors. Though this reduces the hard switching losses, other problems arise. In a practical circuit there will always be small parasitic inductances and capacities. Together with very high current and voltage derivatives, these will create unwanted current and voltage pulses that cause both electromagnetic noise and high component current and voltage stresses as illustrated in Fig. 2(*b*).

The conventional hard switching converter is simple and widely used. The above problems are avoided either by adjusting the switching frequency to an acceptable level, or by derating the device current capability in order not to exceed the acceptable

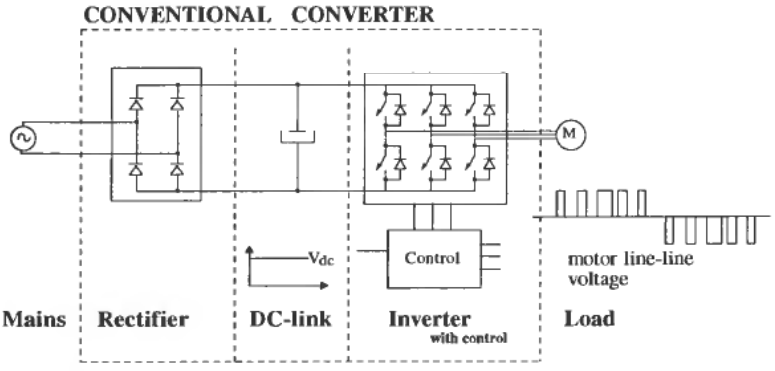
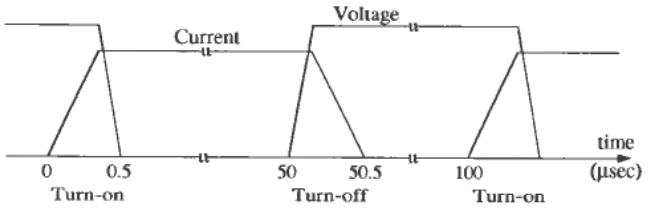
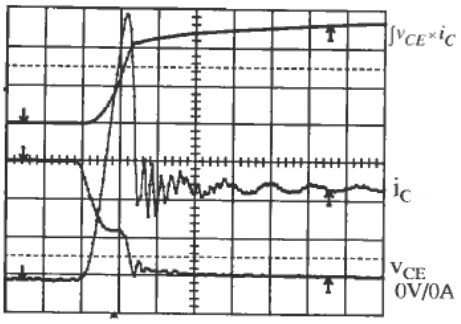


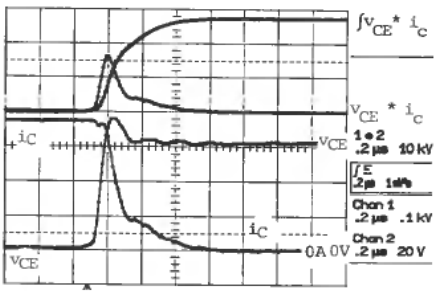
Figure 1. A conventional converter supplying and controlling an a.c. motor.



(*a*)



Turn-on of 25 A.
Transistor current (i_C, 10 A/d)
and voltage (v_{CE})



Turn-off 75 A.
Transistor current (i_C, 20 A/d)
and voltage (v_{CE}).

(*b*)

Figure 2. Transistor current and voltage switching waveforms in turn-on and turn-off. (*a*) Ideal waveforms. (*b*) Realistic switching waveforms together with power dissipated ($i_C \cdot u_{CE}$) and switching losses ($\int i_C \cdot u_{CE}\, dt$) for a 75 A/600 V Toshiba IGBT (MG75J2YS1) at 125°C with $V_{dc} = 300$ V, timescale is 0·2 μsec/div.

switching losses. It is also important to minimize the parasitic inductances and capacitances by using a very good, close mechanical design. The problems however, will always appear when a higher frequency or power is demanded.

2.2. *Soft switching*

The alternative to hard switching is soft switching where the transistor switching losses are strongly reduced. This is done by shaping the transistor currents and/or voltages in a way that makes it possible to switch the transistors at low or zero current and/or voltage. The easiest way to achieve soft switching is by including a snubber (Mohan, Undeland and Robbins 1989) in the conventional converter. Then the power to be dissipated in the transistors is reduced (Petterteig 1991), but the overall converter losses are not lowered.

Another way to achieve soft switching is to use some sort of a resonant converter (Lee, Tbisza and Jovanovic 1989, Divan 1986). In a resonant converter the transistor current and/or voltage is shaped to allow zero current and/or zero voltage switchings. Thus, the overall power losses will be considerably reduced due to strongly reduced switching losses. In addition the nearly square waves of the hard switched converter are replaced by soft sinusoidal waves. In this way the hard switching trade off between switching losses and overvoltages and overcurrents is avoided. On the other hand, most resonant converters introduce higher current and voltage peaks than hard switched converters.

A characteristic of the resonant type converters is the loss of the freedom to switch whenever the controller demands it. Normally it is far more complicated to control a resonant converter than a PWM converter. Resonant converters are often state controlled, with a restricted pulse width and with fixed switching instants.

3. The resonant d.c.-link converter

3.1. *The resonant d.c.-link principle*

The resonant d.c.-link (RDCL) converter (Divan 1986) is one of only a few possible resonant type converters which can be used for a.c. motor drives (Divan and Skibinski 1987; Mertens and Divan 1990). In a resonant d.c.-link converter, the link voltage is made to oscillate at a very high frequency by adding a small capacitor C_{res} and a small inductor L_{res} in the link, as shown in Fig. 3 (*a*). The obtained d.c.-link voltage contains zero voltage intervals and resonant intervals as shown in Fig. 3 (*b*).

By generating zero voltage intervals, it is possible to switch the converter transistors at zero voltage, and thus reduce the switching losses of both the transistors and the freewheeling diodes of the inverter. The most important disadvantages of this approach are complex control, high d.c.-link voltage and high inductor (L_{res}) current stresses.

The converter is allowed to switch only in the zero voltage intervals and the low frequency load voltages are synthesized using whole resonant pulses or absence of pulses. No pulse width modulation is allowed. Thus, a high oscillating link frequency is required in order to obtain good dynamic performance. The link frequency is the frequency of the link voltage oscillations.

In the simulations of the 20 kW converter the link frequency is 60 kHz. In a converter of this size using IGBT transistors a link frequency between 50 kHz and 100 kHz is used. The transistor switching frequency depends on the load condition and the modulation principle, and at a maximum it is half the link frequency, normally much lower.

3.2. *Control of the link oscillations*

The RDCL converter has two control tasks. Like the conventional converter, the inverter has to control the motor currents or voltages. This is done by choosing the appropriate switch states for the resonant voltage intervals, as will be described later.

Another separate and special control task is to control the link voltage and make sure that the oscillations do not fade out (Petterteig, 1992 Chap. 2). This is performed by deliberately shorting the link and controlling the length of the enforced zero voltage interval. The zero voltage interval is forced and controlled in order to maintain the link

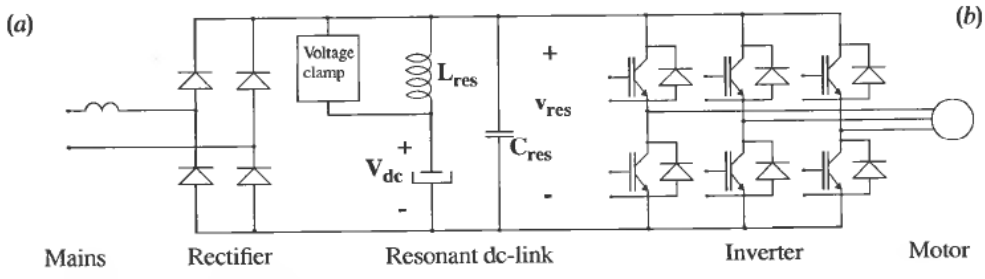


Figure 3. A simplified RDCL converter (*a*) with its oscillating d.c.-link voltage (*b*).

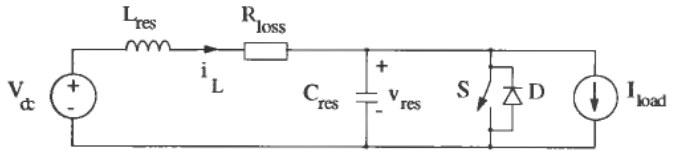


Figure 4. The simplest equivalent circuit for the RDCL converter.

oscillations and make sure that the link voltage reaches zero after every resonant interval. This control is necessary because of resonant circuit losses and instantaneous changes in the total current out of the link (I_{load} in Fig. 4).

Every resonant d.c.-link converter is basically a parallel loaded series resonant circuit as shown in Fig. 4. The resistor R_{loss} represents resonant circuit losses I_{load} equals the total current out of the link and may change in steps in the zero voltage intervals due to switchings of the converter. Each resonant interval starts with zero initial capacitor voltage ($v_{res}=0$), and it is of great importance that the link voltage oscillates back to zero after the resonant interval. If not, the link oscillations will face out.

With zero current ($I_{load}=0$), a small initial inductor current I_{zero} is needed as the resonant interval starts in order to compensate for the resonant circuit losses and make v_{res} oscillate back to zero (Petterteig 1992). With a given load current I_{load}, the inductor current needs to be equal to or greater than $I_{zero}+I_{load}$ as the resonant interval starts, in order to make v_{res} oscillate back to zero. The load current I_{load} may change from one resonant interval to the next due to switchings of the converter. I_{load} is given by the a.c. currents of the inverter and its switch state as shown later in Table 2.

The link voltage is controlled by turning on all the inverter transistors (Fig. 3) and deliberately shorting the link every time the link voltage reaches zero. In this shorted link interval, the inductor current builds up with a di_L/dt equal to V_{dc}/L_{res}. The length of this forced zero voltage interval needs to be actively controlled and a new resonant interval should start as soon as possible when i_L larger than or equal to $I_{zero}+I_{load}$ is detected. In the RDCL circuit where all inverter transistors conduct in each zero voltage interval, the I_{load} valid in the next resonant interval is not measurable in the zero voltage interval and needs to be predicted.

If I_{load} increases, the inductor current needs time to build up to the value $I_{zero}+I_{load(new)}$ and the zero voltage interval will be longer than when I_{load} stays constant. In this case, the inductor current as the next resonant interval starts will be just sufficient to make v_{res} oscillate back to zero. If I_{load} decreases significantly from one resonant interval to the next, the initial inductor current as the resonant interval starts will be much larger than the necessary $I_{zero}+I_{load(new)}$ and the zero voltage interval should be made as short as possible. In this case the large initial inductor current causes the link voltage to significantly exceed the steady state maximum value of $2\times V_{dc}$.

This high maximum link voltage peak cannot be tolerated in practical circuits and the maximum link voltage needs to be limited by a voltage clamp circuit (Petterteig, 1992 Chap. 2). This paper describes a passively clamped circuit (Divan and Skibinski 1987) with a maximum link voltage of $2{\cdot}1\times V_{dc}$. With the maximum voltage most of the excess inductor energy due to the significant reduction (ΔI_{load}) of I_{load} will be transferred to the clamp circuit. This energy is approximately equal to $\frac{1}{2}L_{res}(\Delta I_{load})^2$ (when I_{zero} is much less than ΔI_{load}). If ΔI_{load} is doubled, the energy to the clamp increases four times. In order to minimize this energy transfer to the clamp, ΔI_{load} should be kept as small as possible. This is stressed later in the modulation and simulation part.

The link shorting is state controlled and needs active and fast measurements of the link voltage v_{res} and the inductor current i_L. In addition, this control needs to be fast. Switchings of the converter cause I_{load} to change instantaneously from one resonant interval to the next, which again influences both the link voltage waveforms and frequency. A less time critical measurement of the converter a.c. currents is required in order to be able to control the currents and to be able to calculate the next I_{load}.

4. The circuit simulation program KREAN

In this paper, the simulation program KREAN (Nilssen and Frydenlund 1990; Nilssen and Mo 1990) is used. It is developed at the Norwegian Institute of Technology (NTH) and the Norwegian Electric Power Research Institute (EFI).

KREAN includes a limited number of basic elements like resistors, capacitors, sources, and switches. Circuits are specified in a data file on a nodal basis. Each component is specified by an individual name, the node names to which they are connected, their individual parameters and eventual initial values. KREAN works with variable time steps. The time between two calculations is small in case of switchings or discontinuities. When there are long periods with steady behaviour, the time between two calculations is long.

One important, and here absolutely necessary, feature of KREAN is the ability to make user defined programmable modules (Mo 1991; Mo, Petterteig, Ringheim and Nilssen 1991). They are introduced to enable the user to simulate more advanced circuit elements than what is possible with the standard KREAN version. A KREAN programmable module is a general multiterminal component connected to the circuit as any of the standard components. The module may have nonlinear, dynamic and/or discrete behaviour. It is described by a FORTRAN subroutine, linked to the program by the user, and specified in the datafile on a nodal basis.

In order to be able to simulate the RDCL converter, its control, including the control of both the link oscillations and the converter a.c. currents, has to be implemented as programmable modules. One module is used to control each converter. Several alternative modules are made to control the same converter (Petterteig 1992). With the same inputs and outputs, only the modulation part that chooses the switch pattern is different. To change this control logic is a matter of programming, which makes it relatively easy to change or modify the control.

5. Simulated circuits

Two different RDCL converters are simulated, one single phase mains rectifier and one three phase inverter for induction motor drive (Petterteig and Undeland 1991; Petterteig 1992). The simulations focus on different current control and modulation methods. Important variations are shown in current and voltage waveforms, and in the energy flow to the clamp, due to the different ways of choosing which transistors to conduct. The single phase rectifier is easy to understand and shows the RDCL principle and different events more clearly than the three phase inverter.

Both the rectifier and the inverter are connected to a passively clamped resonant d.c.-link with 400 V constant d.c. voltage (V_{dc}) and a maximum link voltage of 820 V. The average oscillating link voltage frequency is about 60 kHz. The sinusoidal mains and motor current references are given with constant amplitudes and a constant frequency equal to 50 Hz. The control of the d.c.-voltage is not discussed.

The passive clamp, here represented by the diode D_c and the voltage source V_c, limits the maximum link voltage to the level 820 V ($V_{dc} + V_c$). In a practical converter the voltage V_c can be a capacitor with a voltage control unit to keep the capacitor voltage approximately constant and equal to V_c.

5.1. *Single phase rectifier*

The simulated single phase rectifier is shown in Fig. 5. It controls the main current (i_m) to follow its sinusoidal current reference i_{mref} with 90 A rms value and which is in phase with the mains voltage (v_m). This gives a mains power of 20 kW. The same amount of energy is drawn from the link by the 50 A current source which simulates the load. This means that the energy delivered to the clamp circuit due to switchings of the converter has to be drawn from the bulk capacitor C_{dc}, and V_{dc} will decrease slightly in this case where V_{dc} is uncontrolled.

5.2. *Three phase inverter*

Figure 6 shows the simulated three phase inverter. The three a.c. voltage sources v_{xm} (where x is r, s, or t), and inductors L_s represent an induction machine equivalent. The three phase current references i_{xref} are symmetrical, sinusoidal with 50 A rms value, and lags the voltage v_{xm} with 10 degrees. The motor voltage v_{xm} equals 115 V rm, which equals a line to line voltage of 200 V rms. This gives an active motor power of 17·3 kW. The motor frequency is 50 Hz and the motor inductances, L_s, are equal to 1 mH.

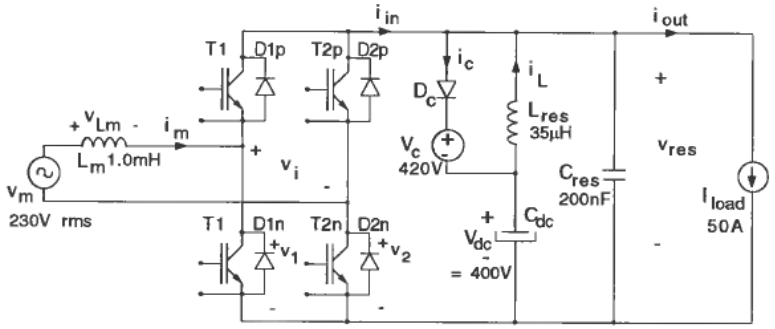


Figure 5. Power circuit for simulating the single phase mains power conditioner.

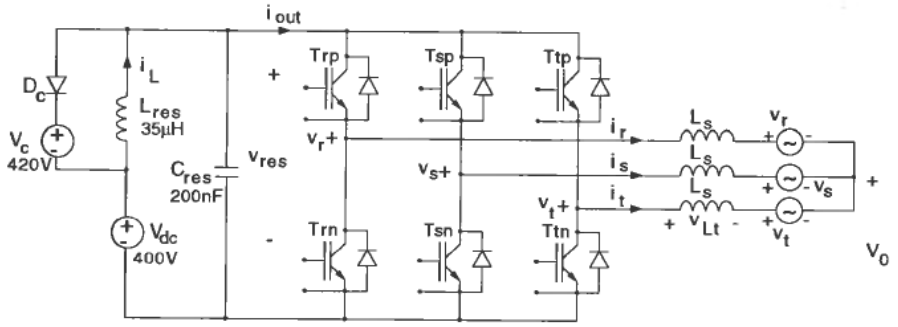


Figure 6. Circuit diagram for the simulations of a three phase inverter with a motor equivalent consisting of inductances and voltage sources. The link is passively clamped.

5.3. *Current control*

Both converters are current controlled by choosing the appropriate switch states for the resonant intervals. In the following, the zero voltage interval conditions are neglected. By changing the switch states that is the pattern of conducting and not conducting transistors, only the a.c. side voltages can be controlled directly. The a.c. currents are indirectly controlled.

The converters consist of two or three vertical bridge legs, i.e. the transistors $T1p$ and $T1n$ with their freewheeling diodes. One and only one transistor in each bridge leg has to be turned on at any time. This gives four possible switch states for the single phase converter and eight different switch states for the three phase converter. This implies that there are several possible ways to make the a.c. currents follow their references. The way of choosing a series of switch states is called a modulation principle.

The following presents different modulation principles for the two converters that are presented and show the influence of the modulation principles on the converter performance. This paper focuses on four performance factors:

(1) The current waveforms compared to the current references.
(2) The changes of current into and out of the link (ΔI_{load}) which gives energy transfer to the clamp and reduces the efficiency of the converter.
(3) The voltage waveforms on the a.c. side of the converters. The harmonic content of these pulsed voltages decides the need for filtering of the mains and also the unwanted motor defects.
(4) The inductor current ripple which causes severe inductor stresses in an RDCL converter.

It will be shown how different modulation methods influence these four performance factors. The two converters are similar in operation, but the single phase converter is much easier to analyse because of its simple structure.

6. The single phase rectifier

6.1. *Control of the single phase rectifier*

The main current (i_m) is controlled to be sinusoidal and in phase with the main voltage (v_m).

In a single phase rectifier there are four different switch states, four possible switch combinations. The voltage v_i (Fig. 5) equals either v_{res}, $-v_{res}$ or zero, depending on the switch state that is chosen. Then the main current derivative is given as follows:

$$\frac{di_m}{dt} = \frac{v_{Lm}}{L_m} = \frac{v_m - v_i}{L_m} \tag{1}$$

When v_m is positive, then i_m can be increased very fast by choosing v_i equal to v_{res}, i_m can be increased slowly by choosing v_i equal to zero, or i_m can be decreased by choosing v_i equal to $-v_{res}$. This gives several alternative ways of obtaining the wanted current waveform.

In the resonant d.c.-link converter, the switch state is allowed to change only in the zero voltage intervals. The pulse width of v_i is therefore a multiple of the resonant period, and v_i can change with a maximum frequency equal to half the resonant frequency. Because of this minimum time between each change in circuit condition, zero tolerance band is chosen for the current modulators.

Three different modulation methods are described in the following using different pattern of v_i to control the mains current. They are described in principle with the focus on performance, not details.

The single pulse width (SPW) modulation, illustrated in Fig. 7, has two switch alternatives:

$i_m > i_{mref}$—$T1p$ and $T2n$ are turned on in the next zero voltage interval

$i_m < i_{mref}$—$T1n$ and $T2p$ are turned on in the next zero voltage interval

Then v_i equals $+v_{res}$ or $-v_{res}$. This modulation method always chooses the highest possible mains current derivatives. This causes frequent switchings, and gives a large ripple current. Another important and negative consequence of using SPW is that i_{in} switches directly between $+i_m$ and $-i_m$ (Fig. 7(*d*)) and is never zero.

The modified single pulse width (MSPW) modulation, illustrated in Fig. 8, has a preferred switch state as in SPW modulation, but the changes in the switch state are restricted. The current into the link (i_{in}) is never allowed to change directly between $+i_m$ and $-i_m$ (Fig. 8). It is forced to be zero for one resonant interval before it is allowed to change direction. Thus, the clamp energy is reduced compared to the single pulse width modulation. Large maximum ripple currents will occur because MSPW chooses the highest possible main current derivative whenever it is allowed to.

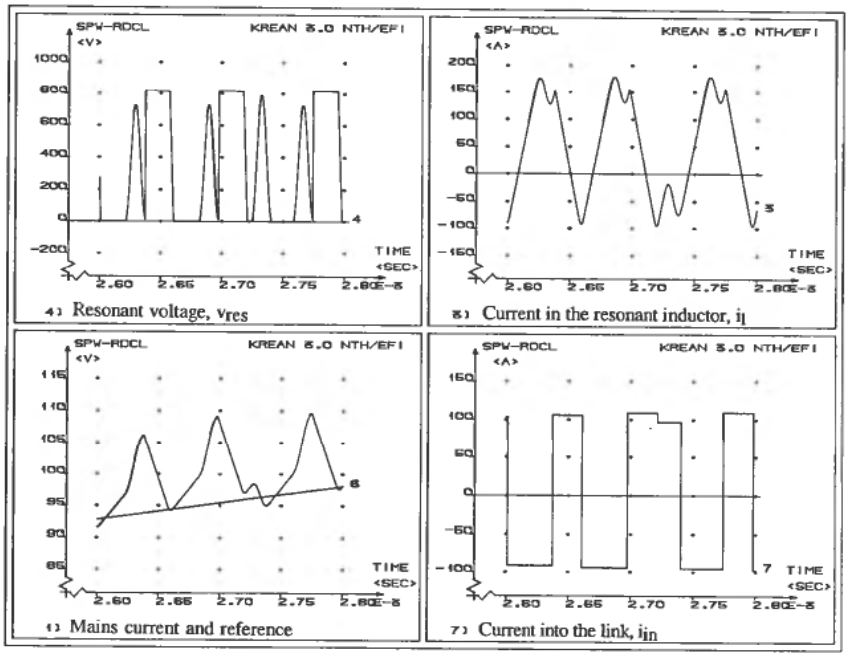


Figure 7. Simulations over 200 μsec with the single pulse width modulation method SPW. Upper left curve, line voltage v_{res}, -200 V to 1000 V, 200 V/d. Upper right curve, current in the resonant inductor i_L, -150 A to 200 A, 5 A/d. Lower left curve, mains current i_m and its reference i_{mref}, 85 A to 115 A, 50 A/d. Lower right curve, current into the link I_{in}, found in the module, 100 A to 150 A, 50 A/d.

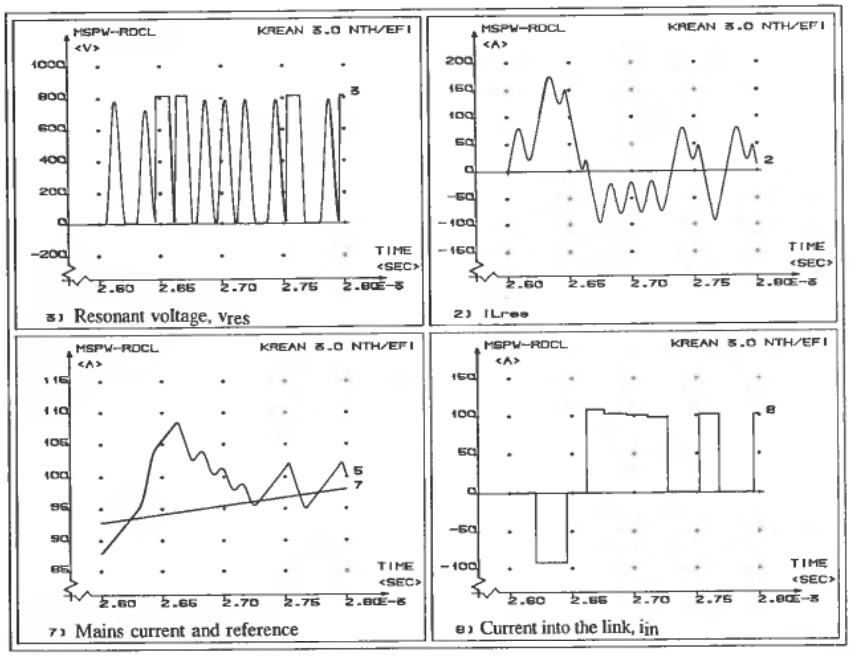


Figure 8. Simulations over 200 μsec with the modified single pulse width modulation method MSPW. Upper left curve, link voltage v_{res}, -200 V to 1000 V, 200 V/d. Upper right curve, current in the resonant inductor i_L, -150 A to 200 A, 5 A/d. Lower left curve, mains current i_m and its reference i_{mref}, 85 A to 115 A, 50 A/d. Lower right curve, current into the link I_{in}, found in the module, 100 A to 150 A, 50 A/d.

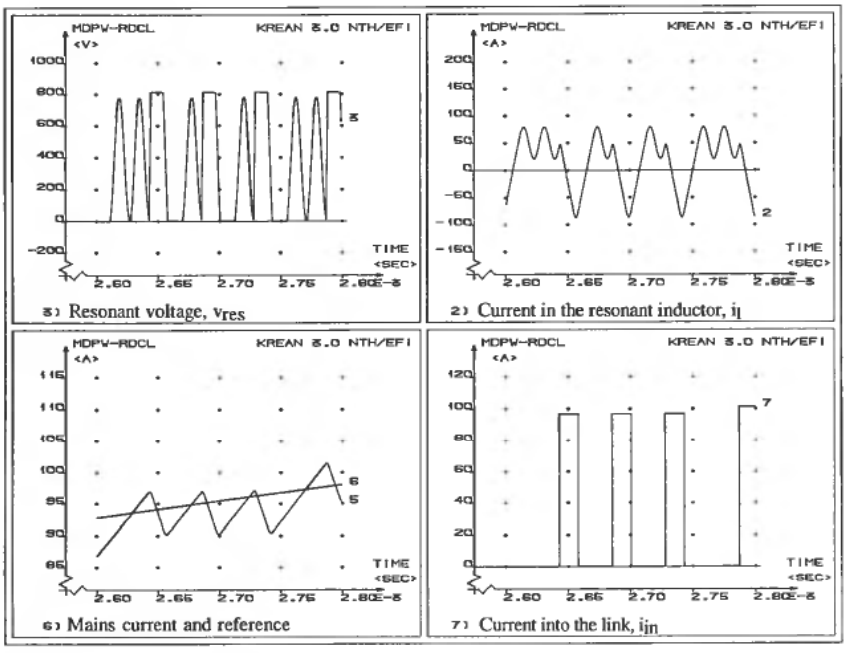


Figure 9. Simulations over 200 μsec—modified double pulse width modulation method MDPW used. Upper left curve, link voltage v_{res}, -200 V to 1000 V, 200 V/d. Upper right curve, current in the resonant inductor i_L, -150 A to 200 A, 5 A/d. Lower left curve, mains current i_m and its reference i_{mref}, 85 A to 115 A, 50 A/d. Lower right curve, current into the link I_{in}, found in the module, 100 A to 150 A, 50 A/d.

The modified double pulse width (MDPW) modulation principle, illustrated in Fig. 9, always chooses the lowest possible current derivative and it never switches i_{in} directly from $+i_m$ to $-i_m$. The voltage v_i is changed between $+v_{res}$ and 0 as long as its fundamental component (v_{i1}) is positive, and between $-v_{res}$ and 0 as long as its fundamental component (v_{i1}) is negative. This means that i_{in} is positive or zero in the entire mains period, except in the short intervals where v_{i1} and v_m have different polarity. This modulation method consistently chooses the smallest possible current derivative. This gives the lowest current ripple of the three modulation methods presented.

When v_{i1} is used as control criteria, the angle of which v_{i1} lags v_m has to be calculated. Alternatively the mains current reference can be used instead of v_{i1} in the modulation method. Then the mains current will be uncontrolled in a short interval around its zero crossing, but the converter control will be easier (Petterteig 1992).

6.2. *Simulation results—single phase rectifier*

The single phase rectifier is simulated over half of the main period with the three different modulation methods (SPW, MSPW and MDPW). Current and voltage waveforms are shown, and the energy transfer to the clamp is calculated. The modulation method MDPW shows the best performance concerning all the four performance factors that were presented previously.

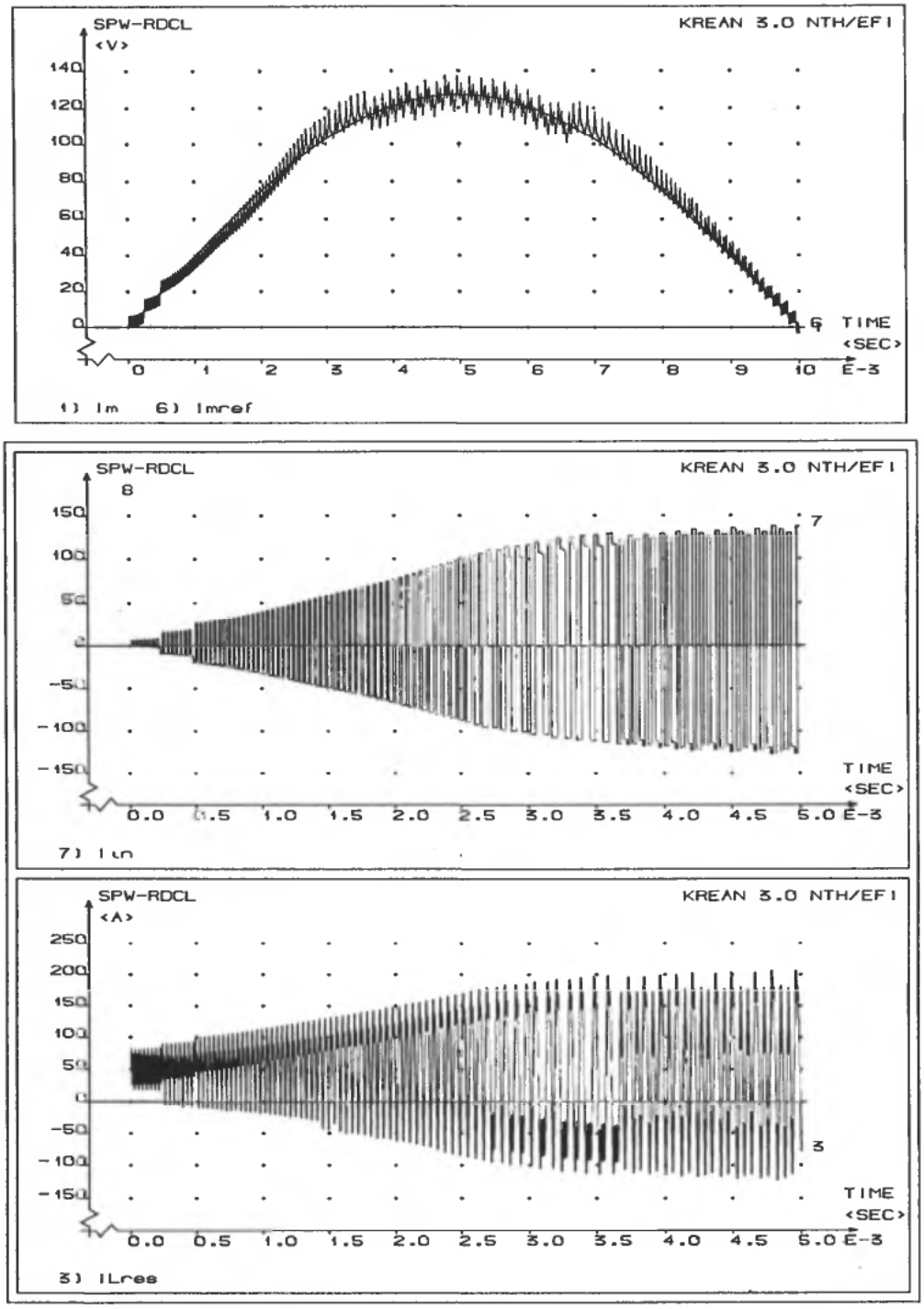
Figure 10 shows main current over half of the main period, 10 msec, with each of the three modulation principles. Figure 10 also shows the current into the link (I_{in}), and the resonant inductor current (i_L), the plotted intervals are 5 msec. I_{in}, calculated inside a KREAN programmable module, is a sampled value of the real current i_{in}.

Table 1 lists average values of i_{mref}, i_m, i_L and i_c, and the mains current rms value, all calculated by KREAN. Table 1 also shows the average power transferred to the clamp, which is important in order to compare the three modulation methods.

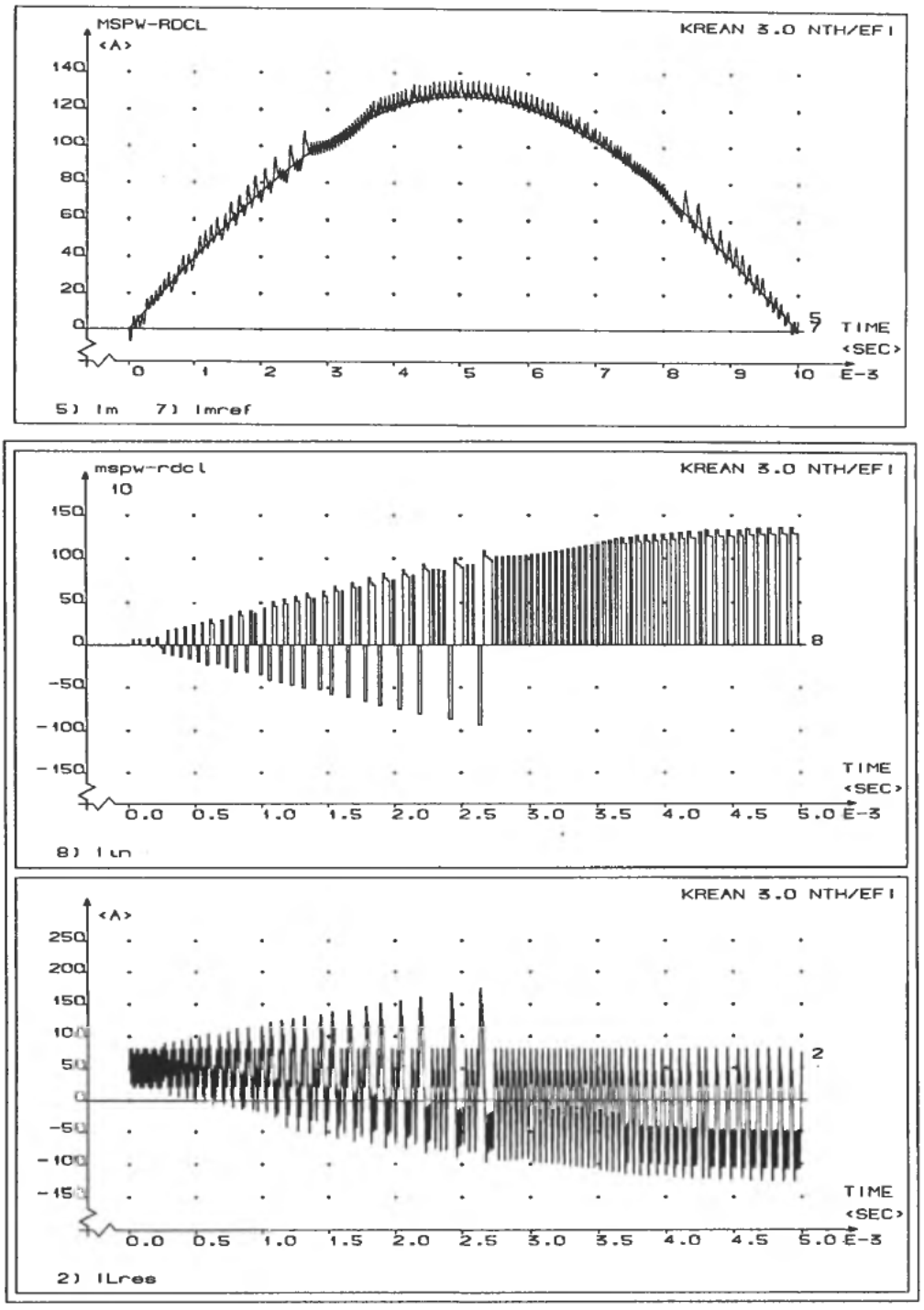
By applying this MDPW modulation method, the harmonic content of v_i is minimized. At the same time, i_{in} is never changed directly from a negative to a positive value, and the power provided to the clamp is minimized. In addition, the resonant inductor current ripple, which causes inductor stresses, is minimized when applying MDPW. These v_i and i_{in} waveforms are achieved by consequently choosing the smallest possible mains current derivative. In the RDCL converter with fixed pulse width, the small current derivatives give lower current ripple than the large current derivatives.

	Single pulse width modulation SPW	Modified single pulse width modulation MSPW	Modified double pulse width modulation MDPW
Average reference current	81 A	81 A	81 A
Average main current	81·5 A	82·7 A	81·4 A
Mains current I_m (rms)	90·7 A	91·8 A	91·0 A
Power supply from the mains	20·8 kW	21·1 kW	20·9 kW
Average clamp current, I_{cm}	−21·9 A	4·8 A	−4·8 A
Mean clamp energy ($I_{cm} \times V_c$)	9·2 kW	2·0 kW	2·0 kW

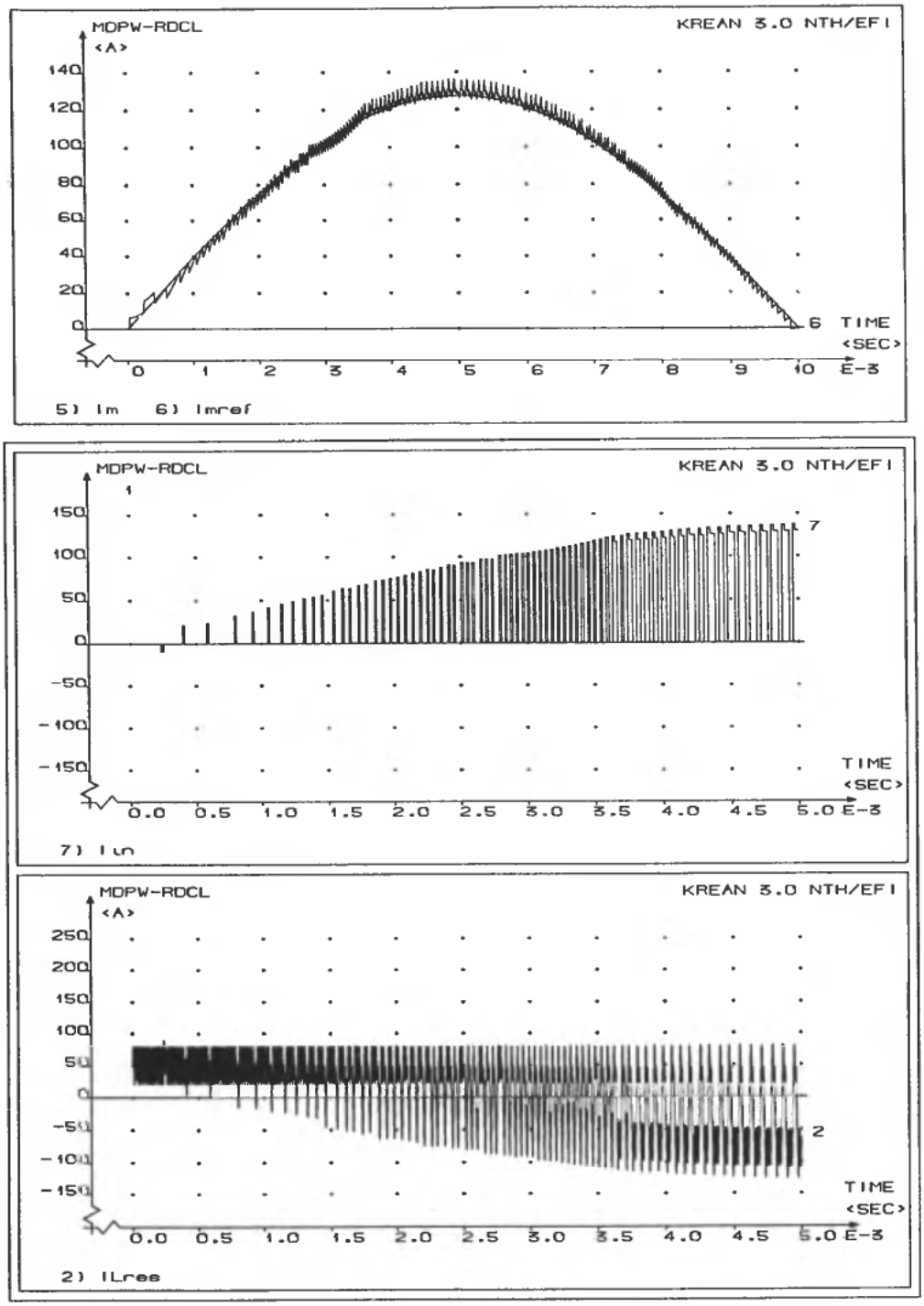
Table 1. Comparison of results from simulations of the single phase mains power conditioner with the three different modulation strategies. $I_{mref} = 90$ A (rms) and $L_m = 1{\cdot}0$ mH. 50 A load current. The average values are calculated by KREAN over a period of 10 msec.



(*a*) Simple pulse width modulation, SPW.



(*b*) Modified simple pulse width modulation, MSPW.



(*c*) Modified double pulse width modulation, MDPW.

Figure 10. A single phase mains power conditioner is simulated with the three modulation principles. $I_{mref} = 90$ A (rms), and $L_m = 1{\cdot}0$ mH. The upper curves show the mains current waveforms (i_a) and reference (i_{mref}). Plot interval: 10 msec. The centre curves show current into the link I_{in} and the lower curves show the resonant inductor current i_L. Note that v_i has the same polarity as I_{in}! Plot interval: 5 msec.

The SPW modulation method consequently chooses the highest possible current derivative. This causes high mains current ripple. When using the SPW modulation method, both v_i and i_{in} change polarity every time the converter switches. Thus, the harmonic content of v_i is large, there is a large power flow to the clamp, and the inductor current ripple is large.

The MSPW modulation method seeks to utilize the highest possible current derivative, but it does not allow i_{in} to change polarity directly. This causes the maximum mains current ripple, when using MSPW, to be the same as when using SPW, but the energy transfer to the clamp is the same as when using MDPW. When looking at the i_{in}, v_i and i_L waveforms, the performance of MSPW is better than the SPW, but worse than the MDPW.

When i_m increases instantaneously, the excess resonant inductor current is approximately equal to the change in i_{in} (ΔI_{in}). The number of switchings of i_{in} are almost the same for all three modulation methods. Compared to the two other methods, SPW has twice the change in current into the link (ΔI_{in}) in each switching. A doubling of ΔI_{in} causes four times larger energy supply to the clamp. Thus, it seem likely that the average power flow to the clamp increases from 2·0 kW when using MDPW or MSPW, to 9·5 kW when using SPW. This large difference is confirmed by the I_{in} current waveforms shown in Fig. 10. The power supplied from the mains is 20 kW in all three cases.

7. The three phase inverter

7.1. *Control of the three phase inverter*

Table 2 shows the eight switch states, $k = 0, 1, 2, .. 7$, with the corresponding voltages applied to the load and current drawn from the d.c.-link. S_r, S_s and S_t are the control signals for each bridge. $S_x = 1$ means that the upper transistor in bridge x is on (x is r, s or t). $S_x = 0$ means that the lower transitor in bridge x is on. States 0 and 7 are zero states where no energy is transferred to or from the output.

A conventional PWM control strategy cannot be used in the RDCL converters where all switchings are synchronized to the zero voltage intervals of the d.c.-link voltage. In literature the family of delta modulators is presented as ideally suited for the control of resonant link converters (Kheraluwala and Divan 1987, 1988; Habetler and Divan 1988).

k	S_r	S_s	S_t	V_0	I_{out}	$V_r - V_0$	$V_s - V_0$	$V_t - V_0$
0	0	0	0	0	0	0	0	0
1	1	0	0	$\frac{1}{3}v_{res}$	i_r	$\frac{2}{3}v_{res}$	$-\frac{1}{3}v_{res}$	$-\frac{1}{3}v_{res}$
2	1	1	0	$\frac{2}{3}v_{res}$	$-i_t$	$\frac{1}{3}v_{res}$	$\frac{1}{3}v_{res}$	$-\frac{2}{3}v_{res}$
3	0	1	0	$\frac{1}{3}v_{res}$	i_s	$-\frac{1}{3}v_{res}$	$\frac{2}{3}v_{res}$	$-\frac{1}{3}v_{res}$
4	0	1	1	$\frac{2}{3}v_{res}$	$-i_r$	$-\frac{2}{3}v_{res}$	$\frac{1}{3}v_{res}$	$\frac{1}{3}v_{res}$
5	0	0	1	$\frac{1}{3}v_{res}$	i_t	$-\frac{1}{3}v_{res}$	$-\frac{1}{3}v_{res}$	$\frac{2}{3}v_{res}$
6	1	0	1	$\frac{2}{3}v_{res}$	$-i_s$	$\frac{1}{3}v_{res}$	$-\frac{2}{3}v_{res}$	$\frac{1}{3}v_{res}$
7	1	1	1	v_{res}	0	0	0	0

Table 2. The eight switch states with corresponding voltages, and current drawn from the d.c.-link.

The delta modulator is a uniformly sample bang-bang control with zero hysteresis. It must be noted that in the RDCL converter it is not possible to vary the switching duration as in a PWM alternative.

Two methods of sigma delta modulated current control of the three phase converter are presented. These methods use only the necessary feedback of motor currents. In the simplest delta modulator (INVSDM), each phase is switched independently of the others. A better solution seen from the link is to use a modified delta modulator (INVMSD) which restricts the switchings, and minimizes the instantaneous changes in energy flow to and from the link.

A third and more intelligent current control method (INVCON) is also presented using only the same necessary feedback of two motor currents. This method estimates very roughly the motor voltage, v_{xm} in Fig. 6, and considers all three phases together when choosing the switch state. To be able to choose the apparently best switch pattern, it is necessary to use a more accurate motor voltage, this is difficult to find since motor parameters must be calculated or measured.

The current regulated delta modulator here called INVSDM (Habetler and Divan 1988) switches the three bridge legs independently of each other, and is the easiest strategy for the control of an RDCL converter. The INVSDM always chooses the state which drives all the three phase currents in the right direction as fast as possible, with a maximum rate of current change. If the measured current i_x in phase x, is greater than its reference value (i_{xref}), then the lower transistor T_{xn} is turned on ($S_x=0$). If the measured current is less than its reference, then the upper transistor T_{xp} is turned on ($S_x=1$).

The INVSDM will never choose any zero state, and therefore the current drawn from the link i_{out} (Fig. 6) might change instantaneously from positive to negative and vice versa. This instantaneous reversal of the link current causes a stressed link operation.

The modified current regulated delta modulated controller here called INVMSD (Habetler and Divan 1988) never allows the current out of the link to change polarity directly. The wanted next switch state is chosen like in the INVSDM, but the allowed switchings are restricted. The only state transitions allowed are those between adjacent states and zero. Adjacent states are where only one of the control signals, S_a, S_b or S_c changed. One of the zero states are chosen when a change in current is wanted in more than one of the phases. After a zero state, any wanted switch state may be chosen. Table 3 shows how the next switch state is chosen, when the previous and the wanted switch states are known.

Wanted next state	Previous state						
	0	1	2	3	4	5	6
1	1	1	1	0	0	0	1
2	2	2	2	2	0	0	0
3	3	0	3	3	3	0	0
4	4	0	0	4	4	4	0
5	5	0	0	0	5	5	5
6	6	6	0	0	0	6	6

Table 3. The allowed selected next state, given by the previous state and the wanted state. Presented by Habetler and Divan, 1988.

The more intelligent current control method called INVCON estimates the motor voltages v_{xm} and considers the three phases together in order to get best possible current derivatives. The switchings are restricted in order to avoid that the current i_{out} change polarity directly.

In a three phase system, the neutral point of the motor floats with a voltage level depending on the switch state of all three phases. The voltage V_0 (Fig. 6) equals:

$$V_0 = \tfrac{1}{3}(V_r + V_s + V_t) \tag{2}$$

V_x is the voltage applied to the motor phase x referred to the negative link voltage (Fig. 6). V_x equals 0 or v_{res}.

As the switch state cannot directly control the phase currents, the voltage across the inductance L_s, decide the current change. To choose a well motivated or 'optimum' switch state, the phase current derivatives in the next resonant period have to be considered:

$$\frac{di_x}{dt} = \frac{v_{Lx}}{L_s} = \frac{1}{L_s}(v_x - V_0 - v_{xm}) \tag{3}$$

The motor inductance, L_s, per phase is assumed known. Then, to be able to tell the current derivatives due to different switch states, it is necessary to know the voltage v_{xm} behind the inductance. This voltage represents the motor flux and the speed, and can not be measured. But b_{xm} can be calculated with a good knowledge of motor parameters and motor conditions. INVCON uses another possibility and calculates a very rough approximated value v'_{xm} of this voltage:

$$v'_{vm} = V_{xl} - V_{0l} - \frac{L_s}{\Delta t} \cdot (I_x - I_{xl}) \tag{4}$$

I_x is the measured phase current in the actual zero voltage interval, and I_{xl} is the measured phase current from the last zero voltage interval. V_{xl} and V_{0l} are average values of V_x and V_0, between the two samples. V_0 is approximately 0, $\frac{1}{3}V_{dc}$, $\frac{2}{3}V_{dc}$, or V_{dc} depending on the switch state. The time Δt can be measured as the time between the actual and the last sample. INVCON, however, uses a constant Δt equal to the resonant period of the link.

The phase current will reach its reference value at the end of the next resonant period if the voltage applied across the inductor equals:

$$L_s \cdot \frac{(I_{xref} - I_x)}{\Delta t}$$

Then the rate of current change is not larger than necessary. In the RDCL converter this is preferable because the derivative of the current in one phase might not be allowed to change polarity in the next resonant interval, not even if the current deviation is large, due to restrictions in the switchings.

To get the wanted current derivative, V_x and V_0 must be given by:

$$S_{xw} = V_x - V_0 = L_s \cdot \frac{(I_{xref} - I_x)}{\Delta t} + v'_{xm} \tag{5}$$

The possible values, however, according to the switch states, $S_{xk} = V_x - V_0$, are shown in Table 2. A cost function is calculated for each switch state k:

$$C_k = \text{abs}(S_{rw} - S_{rk}) + \text{abs}(S_{sw} - S_{sk}) + \text{abs}(S_{tw} - S_{tk}) \tag{6}$$

where k is an index running through all switch states that are allowed (Table 2). The allowed states include the present state, the adjacent states and one zero state. Among the allowed states, the state with the lowest cost function is chosen as the next state. In this way the differences between actual current and its reference value in all three phases are taken care of and minimized.

This control method is better, but also more expensive, than the modulation methods INVSDM and INVMSD. The calculations of the cost functions C_k which have to be carried out in every zero voltage interval are time consuming for a micro controller. The calculation of v'_{xm} can be done for instance only twenty times for each period of the motor voltage because v_{xm} changes slowly compared to the link frequency.

7.2. *Simulation of the three phase inverter*

The three phase inverter is simulated over 20 msec (which is one period of the motor frequency) using the three different modulation and control methods (INVSDM, INVMSD and INVCON). Figure 11 shows the current in one phase i_r and the line to line voltage v_{rs} over 10 msec. Table 4 shows the calculated rms and fundamental value of i_r and also the calculated power flow to the clamp. INVCON is shown to be best when considering motor current ripple, current harmonics and line to line voltage waveforms. INVMSD is shown to be better when the power flow into the clamp is considered. Despite its simpleness INVMSD shows good overall performance.

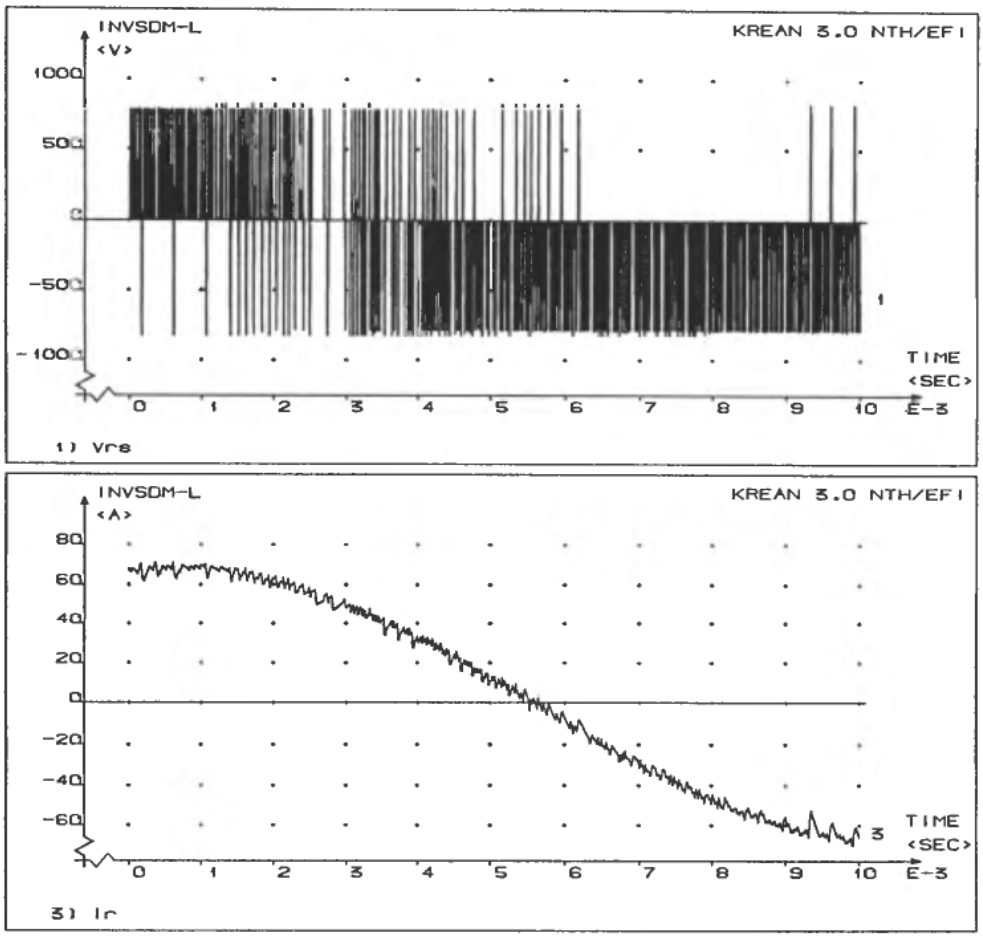
Figure 11 illustrates that the fastest possible change in current is not the best. This is common for most converters, but it is more important in RDCL converters than in PWM converters for two reasons. In an RDCL converter the pulse width is fixed and the switch condition cannot be changed before next zero voltage interval, even if the controlled current is out of range. In most three phase RDCL converters the modulation method restricts the switchings and normally allows only one bridge to switch at a time. Depending upon the modulation method, the phase that is allowed to change is not always the one with the highest current deviation.

INVSDM treats all phases separately when choosing switch state, and allows all switch states. The result is large current ripple and large power flow to the clamp. INVMSD treats all three phases separately when finding the wanted switch state (like INVSDM), but restricts the switchings in order to avoid that i_{in} changes polarity directly. The result is a much better current performance than INVSDM, but higher current ripple than INVCON.

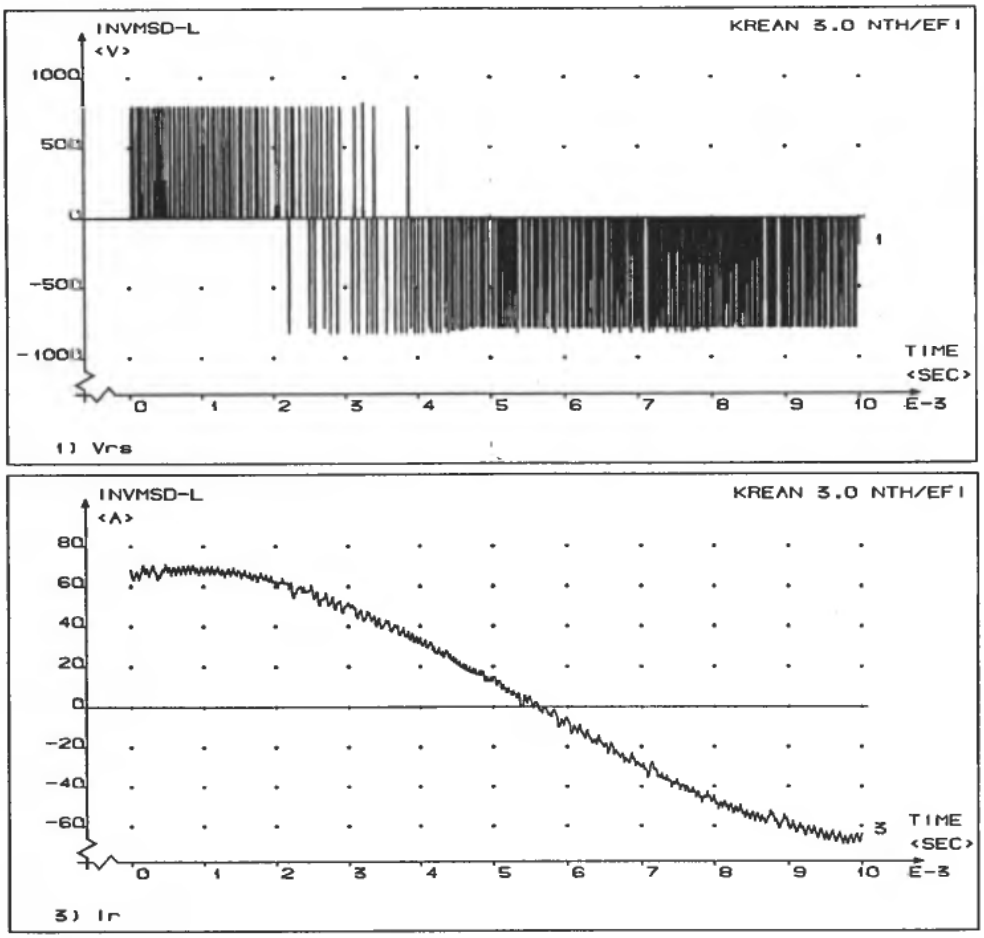
All three methods have a fundamental mains current that is more than 99·6% of the mains current rms value (Table 4). Thus, the higher harmonic components are insignificant. INVSDM has the lowest mains current rms value (47·22 A), INVCON has the highest (49·73 A). The mains current reference is 50 A rms.

	INVSDM	INVMSD	INVCON
I_r–rms phase current	47·22 A	47·80 A	49·37 A
I_{r1}–fundamental phase current	47·07 A	47·72 A	49·71 A
$I_{c,av}$—average clamp current	1·60 A	1·12 A	1·46 A
Average power flow into the clamp ($V_c \times I_{c,av}$)	670 W	470 W	610 W

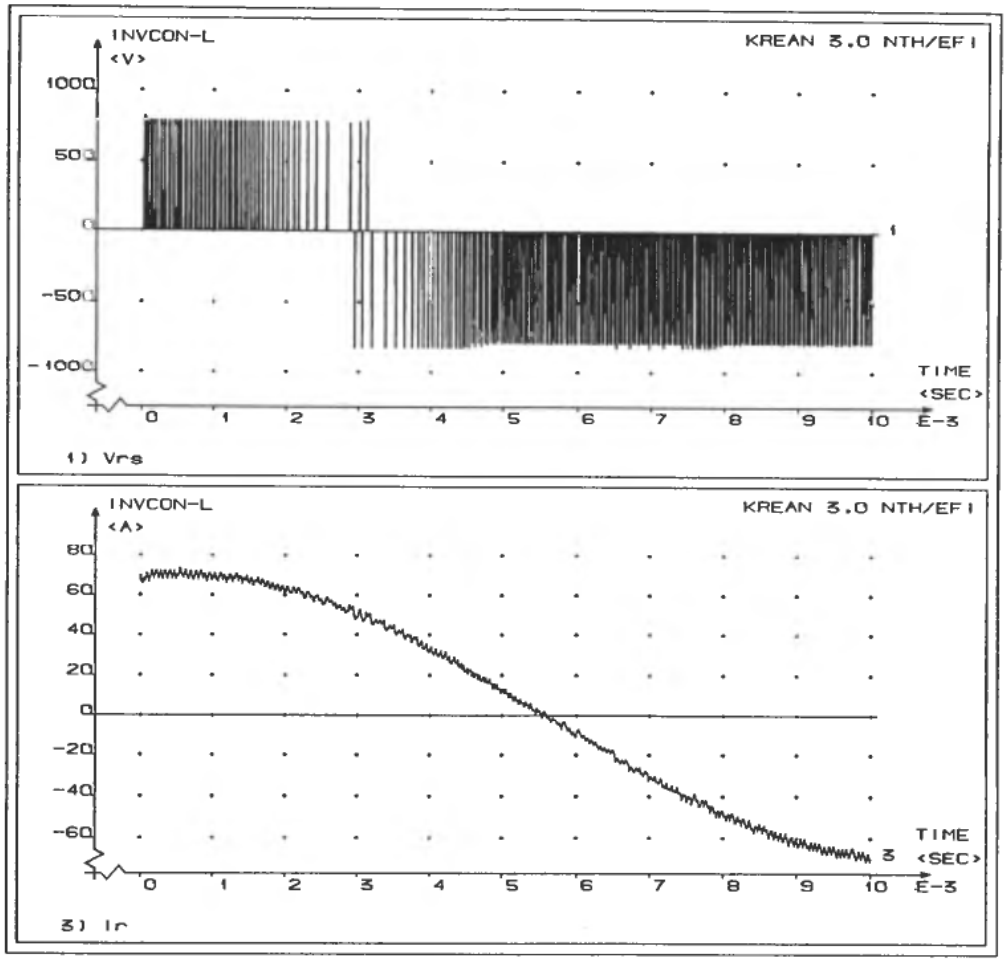
Table 4. Results from analysis of the simulations using INVSDM, INVMSD and INVCON. The mains current harmonics are calculated over a 20 msec period, $I_{c,av}$ over a 10 msec period.



(*a*) INVSDM used for control.



(*b*) INVMSD used for control.



(*c*) INVCON used for control.

Figure 11. Simulations over 10 msec (half the period) using different control methods, upper curves, phase to phase voltage v_{res} −1000 V to 1000 V, lower curves, phase current i_r, −60 A to 80 A (20 A/div).

Considering current ripple, phase current harmonics and line to line voltage, INVCON shows the best performance. INVSDM definitively shows the worst performance, and the performance of INVMSD is somewhere between the two others.

When the power flow into the clamp is considered, INVMSD is best. This method gives the lowest power to the clamp, 470 W. The active power supplied to the motor in this case is 17 kVA. The method INVCON has an unexpectedly large power flow to the clamp, 610 W, which is 30% more than INVMSD. The INVSDM supplies most power to the clamp, 670 W which is 43% more than the INVMSD. INVSDM has the highest power flow into the clamp because it allows i_{in} to change polarity directly.

8. Conclusions

The simulations show that the modulation method essentially influences the overall performance of the resonant d.c.-link converter. It is shown that the switchings

should be restricted to avoid that the current into or out of the d.c.-link changes polarity directly and causes a too large power flow to the voltage clamp.

In the single phase rectifier, the SPW modulation method is shown to be the worst. The MDPW modulation method is absolutely superior to the others for several reasons (Fig. 10 and Table 1):

- With MDPW, the mains current has the lowest current ripple
- With MDPW, the voltage v_i (Fig. 5) has the lowest harmonic distortion
- MDPW has the smallest power flow into the voltage clamp, 10% of supplied power
- MDPW has the lowest inductor current ripple

For the three phase inverter, the current control method INVCON is shown to be best when considering motor current ripple, current harmonics and line to line voltage waveforms (Fig. 11). The current modulation method INVMSD is shown to be best when the power flow into the clamp is considered (Table 4). Despite its simplicity, INVMSD shows good overall performance.

References

BOSE, B. K. (1989). Power electronics—an emerging technology, *IEEE Transactions on Industrial Electronics*, **36**, 403–412.

DIVAN, D. M. (1986). The resonant d.c.-link converter—A new concept in static power conversion, *IEEE-IAS Annual Conference Records*, pp. 648–656.

DIVAN, D. M. and SKIBINSKI, G. (1987). Zero switching loss inverter for high power applications. *IEEE Industrial Applications Society Annual Meeting*, pp. 627–634.

HABETLER, T. G. and DIVAN, D. M. (1988). Performance characterization of a new discrete pulse modulated current regulator. *IEEE Industrial Applications Society Annual Meeting*, pp. 395–405.

KHERALUWALA, M. and DIVAN, D. M. (1987). Delta modulation strategies for resonant link converters. *IEEE PESC Conference Records*, pp. 163–169.

KHERALUWALA, M. H. and DIVAN, D. M. (1988). Optimal discrete pulse modulation waveforms for resonant link inverters. *IEEE 1988, PESC Conference Record*, pp. 567–574.

LEE, F. C., TABISZA, W. A. and JOVANOVIC, M. M. (1989). Recent developments in high-frequency quasi-resonant and multi-resonant converter technologies. *European Conference on Power Electronics and Applications, Aachen*, pp. 401–410.

MERTENS, A. and DIVAN, D. M. (1990). A high frequency resonant d.c.-link inverter using IGBTs. *IPEC Conference Tokyo*, pp. 152–160.

MO, O. (1991). *KREAN Module reference manual.* The Norwegian Institute of Technology (NTH) and Norwegian Electric Power Research Institute (EFI).

MO, O., PETTERTEIG, A., RINGHEIM, N. A. and NILSSEN, R. (1991). Application of programmable modules in simulation of power electronics. *European Conference on Power Electronics and Applications, Firenze*, Vol. 4, pp. 396–401.

MOHAN, N., UNDELAND, T. M. and ROBBINS, W. (1989). *Power Electronics: Converters, Applications and Design* (John Wiley & Sons).

NILSSEN, R. and FRYDENLUND, S. (1990). *Reference manual. KREAN main program, Version 3.0, Edition 1.0*, The Norwegian Institute of Technology (NTH) and Norwegian Electric Power Research Institute (EFI).

NILSSEN, R. and MO, O. (1990). KREAN, a new simulation program for power electronic circuits, *IEEE PESC Conference, San Antonio, Texas*, pp. 506–511.

PETTERTEIG, A. (1991). IGBT Turn-off losses in hard switching and with a capacitive snubber. Technical Report No. TR 3854, Norwegian Electric Power Research Institute (EFI).

PETTERTEIG, A. (1992). Development and control of a resonant d.c.-link converter for multiple motor drives. Dr. ing. thesis, The Norwegian Institute of Technology 1992:10, NTH Trykk, ISBN 82-7119-359-7.

PETTERTEIG, A. and UNDELAND, T. M. (1991). Control of a resonant converter with high mains power factor—the need for a powerful simulation tool. *European Conference on Power Electronics and Applications, Firenze*, Vol. 4, pp. 378–383.